IN THE UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
WACO DIVISION

SOLAS OLED LTD.,	)	
Plaintiff	)	
v.	)	Case No. 6:19-cv-00631-ADA
HP INC.,	)	
Defendant.	)	

DECLARATION OF DR. JERZY KANICKI REGARDING CLAIM CONSTRUCTION

1. I, Dr. Jerzy Kanicki, declare as follows:

I. INTRODUCTION

2. I have been retained by HP, Inc. ("HP") as an independent expert consultant in connection with the above-captioned lawsuit to provide my analyses and opinions in certain technical aspects of this dispute.

3. The general purpose of this Declaration is to analyze and explain how a person of ordinary skill in the art at the time of the alleged inventions would understand the technical subject matter of U.S. Patent No. 7,499,042 ("'042 Patent"), U.S. Patent No. 7,573,068 ("'068 Patent"), and U.S. Patent No. 7,663,615 ("'615 Patent") (collectively, the "Asserted Patents"), and whether a person of ordinary skill in the art would understand with reasonable certainty the meaning and scope of certain terms of the '615 Patent. My opinions and the bases for my opinions are set forth below.

4. I am being compensated at my ordinary and customary consulting rate of $450 per hour for my work. My compensation is in no way contingent on the nature of my findings, the presentation of my findings in testimony, or the outcome of this or any other proceeding. I have no other interest in this proceeding.

5. I am competent to testify to the matters stated in this Declaration, have personal knowledge of the facts and statements herein, and each of the statements is true and correct.

II. BASIS FOR OPINION

A. Qualifications

6. I have summarized in this section my educational background, career history, publications, and other relevant qualifications. A more detailed account of my work experience, qualifications, and publications is included in my curriculum vitae, attached as Exhibit A to this declaration.

7. As reflected in my curriculum vitae (and as explained in more detail below), I have experience with the technology described in the ’042, ’068, and ’615 Patents, including thin film transistors, display driving circuits, and OLED technology. The following paragraphs provide a brief summary of my qualifications.

8. I am currently a Professor in the Department of Electrical Engineering and Computer Science (EECS) at the University of Michigan, Ann Arbor, Michigan. I have studied, taught, and practiced in flat panel displays (FPDs) and integrated circuits (ICs) fabrication for over 25 years, including design, thin film depositions, processing, fabrication, and photolithography of devices and circuits used in both applications. The flat panel displays include, for example, active-matrix liquid crystal displays, (AM-LCDs), active-matrix organic light emitting displays (AM-OLEDs) and other light transmissive, reflective and emitting display technologies. I received my Doctorate of Science (D.Sc.) from the Free University of Brussels, Belgium in 1982. My educational background also includes a B.S. (1976) and M.S. (1978) in Chemistry from the Free University of Brussels, Belgium.

9. Since 1995, I have been a member of the faculty at the University Of Michigan College Of Engineering, Ann Arbor, Michigan. During that period, I have held the position of Professor in the Department of Electrical Engineering and Computer Science. Between 1995 and 1999, I was group team leader within the University of Michigan Center of Display Technology and Manufacturing (DTM). The DTM was created to develop FPDs technologies that could be commercialized by local companies to diversify from automotive industry. One of such company was Ovonic Imaging Systems (OIS) located in Northville, Michigan. For number of years, I also held the position of Professor in the Program of Macromolecular Science and Engineering (2000-2011), and Applied Physics (2000-now). During my tenure at the University

of Michigan, I have conducted leading work on various flat panel displays, device and circuit fabrication technologies, including, for example, design for various devices and integrated circuits to be used with flat-panel displays (active-matrix arrays, data and gate drivers chips, and associated electronics), x-ray and optical imagers (pixel circuits, driving and readout chips, and associated electronics), chemical sensors (readout chips), solar cells (DC/AC converters), and fingerprint sensors (driving circuits and readout chips). As a faculty member, over the years I have graduated a number of PhD dissertations in the field of flat panel displays, semiconductor devices and circuits. Upon graduation, my PhD graduate students have moved either into industrial positions in the displays and electronics industries or into academic positions in the U.S. or abroad.

10. I have taught a number of different courses at the undergraduate and graduate levels, including Solid-State Technology Laboratory and Digital Integrated Circuit Technologies, within the EECS department at the University of Michigan. These courses have generally covered the physics, technology, design, and fabrication of solid-state devices and integrated circuits. I have also introduced two new courses, including "Flat Panel Displays" and "Thin Film Devices Technology" in 1997, which are still being offered annually. These courses have generally, covered the thin-film devices and circuits technologies used in different applications including AM-OLEDs. As a faculty member, I direct at any given time the research of several graduate and undergraduate students in Solid-State Devices and Nanotechnology, including semiconductors, electronic materials, devices, and circuits for various applications including FPDs. As part of my group research, I utilize the University of Michigan Lurie Nanofabrication Facility (LNF), https://lnf.umich.edu/, that has the capability to fabricate and test devices and circuits used in the FPDs and IC industries. Moreover, over the years I have also supervised the

research of several post-doctoral fellows and visiting scientists from FPDs and ICs industries or/and other universities within my group doing research in the area of the solid-state devices and circuits. More information about my professional activities can be found on my research group web page: www.eecs.umich.edu/omelab/.

11. From 2002 to 2003, I was on sabbatical at the University of California Santa Barbara (UCSB) within the Center for Polymers and Organic Solids. My research was related to organic polymer thin-film transistors, organic light-emitting devices and electrically injected lasers. During my stay, I supervised research of three graduate students working in these areas. My host was Professor Alan J. Heeger from Physics Department. He won the Nobel Prize for Chemistry in 2000 along with *Alan* G. MacDiarmid and Hideki Shirakawa "for their discovery and development of conductive polymers."

12. From 2009 to 2010, I was on sabbatical at the University of California San Diego (UCSD) within the California Institute for Telecommunications and Information Technology. My research was related to organic polymer thin-film transistor chemical sensors, amorphous InGaZnO thin-film transistors, image sensors and solar cells. During my stay, I collaborated with the number of local companies including Qualcomm and Applied Materials. My host was Professor Andrew C. Kummel from Department of Chemistry and Biochemistry.

13. From 2018 to 2019, I was on sabbatical at the Massachusetts Institute of Technology within Microsystems Technology Laboratories. My research was related to hydrogenated diamond devices and circuits, and Perovskites materials based opto-electronic devices. During my stay, I collaborated very closely with the MIT Lincoln Laboratory. My host was Professor Jesus del Alamo from Department of Electrical Engineering and Computer Science.

14. From 1983 to 1995, I was a Research Staff Member at the IBM T.J. Watson Research Center in Yorktown Heights, New York, involved in the research and development of flat panel display materials, devices, circuits, driving electronics, and manufacturing methods. During that period, I was a member of a team that developed the first IBM active-matrix liquid-crystal displays (AM-LCDs) manufacturing technology, leading to the introduction of the first color laptop computer (CL57-SX) on March 24, 1992. I, among others, was also responsible at IBM for the initial fundamental understanding of device physics and pixel design approaches used for, and manufacturing methods of, certain AM-LCDs for IBM's ThinkPad laptop computers.

15. I am a member of several professional organizations including the Society for Information Display (SID) and the Institute of Electrical and Electronics Engineers (IEEE). My areas of expertise include chemistry, solid-state physics, material sciences, device physics, circuits, solid-state device and circuit fabrication / manufacturing methods, and nanotechnology. I have edited or co-edited several books, authored over 300 technical papers, and given over 350 presentations (among which over 70 were invited presentations) relating to thin film semiconductor devices, circuits, and associated FPD technologies. My papers have received over 10,000 citations, and I have an H-index of 51, i10-index of 167 and RG score of 42.30. I have also been the chair or co-chair at numerous national and international FPD conferences and symposia. I was an editor for IEEE Transactions on Electron Devices for eight years, and I am a reviewer for several prestigious international archival journals. I am also a reviewer of proposals for several federal agencies, such as the National Science Foundation (NSF), Department of Defense (DoD), and Defense Advanced Research Program Agency (DARPA). Among other distinctions, I was awarded the IBM External Honors, which recognizes the technical leadership

of staff members in IBM's Research Division, three times. My research work at the University of Michigan has been supported by grants from the state of Michigan, federal agencies, and a number of international industries.

16. Through my experience and education, I am familiar with most aspects of the manufacturing processes and circuits used in the flat panel displays and integrated circuits industries, including thin film deposition, etching chemistry, chemical mechanical polishing, devices and circuits processing, and photolithography, as they relate to device and circuit fabrication, applications and/or operations. My latest curriculum vitae, and a list of my publications and presentations, is appended as Ex. A.

17. In the previous five years, I have testified as an expert at trial or by deposition or have submitted declarations in the following cases:

- 2018&2017: Xperi Corp. v. Samsung Electronics Co., Ltd.: Latham & Watkins LLP (consultant and expert witness for Xperi Corp.);
- 2016: AU Optronics Inc. v. ShenZhen China Star Optoelectronics Technology Co. Ltd.: Sughrue Mon PLLC (consultant and expert witness for AU Optronics);
- 2016&2017: Eidos Display, LLC et al. v. AU Optronics Corp. et al., Case No. 6:11-cv-00201-JRG-JDL (E.D. Tex.): Jeffer Mangels Butler & Mitchell LLP (consultant and expert witness for defendant);
- 2015: MiiCs & Partners, America, Inc. and Gold Charm Limited v. Toshiba Corporation, Toshiba America, Inc., and Toshiba America Information Systems, Inc., Case No. 1:14-cv-00803-RGA (D. Del.): Dorsey & Whitney LLP (consultant and expert witness for Toshiba Corp. and Toshiba America Information Systems, Inc.);

- 2014: Tessera Intellectual Property Corp., and its subsidiary Invensas Corp. (TIPC) v. Micron Technology and Elpida Memory, Inc.: Latham & Watkins LLP (consultant and expert witness for TIPC).

B. Materials Considered

18. As part of my preparation for writing this Declaration, I reviewed the '042, '068, and '615 Patents and their prosecution histories, the parties' proposed constructions, as well as the documentation identified by the parties in their identifications of intrinsic and extrinsic evidence.

III. LEGAL STANDARDS FOR CLAIM CONSTRUCTION

A. Claim Construction

19. I understand that the words of a claim are generally given the ordinary and customary meaning that the term would have to a person of ordinary skill in the art at the time of the invention.

20. I understand that to determine how a person of ordinary skill would understand a claim term, courts may consider both "intrinsic" and "extrinsic" evidence. I understand that courts look first to the intrinsic evidence of record, which includes the patent itself (including the claims and specification) and the prosecution history. I also understand that courts may consider extrinsic evidence, such as expert and inventor testimony, dictionaries, and learned treatises.

21. I understand that a person of ordinary skill in the art is deemed to read the claim term not only in the context of the particular claim in which it appears, but also in the context of the entire patent, including the specification and prosecution history. Thus, any explicit definitions of terms or intentional disclaimers or disavowals of claim scope in the specification or prosecution history must be considered in determining the meaning of a claim term.

22. I understand that particular embodiments appearing in the written description do not limit claim language that has broader effect, and that the scope of the claims is not necessarily limited to inventions that look like the ones shown in the figures and described in the specification. However, I also understand that the patentee is required to define precisely what he claims his invention to be, and the claims must be construed in a manner consistent with the specification.

23. I am informed that a term must be interpreted with a full understanding of what the inventors actually invented and intended to include within the scope of the claim as set forth in the patent itself. Thus, claim terms should not be broadly construed to encompass subject matter that, while technically within the broadest reading of the term, is not supported when the claims are viewed in light of the invention described in the specification.

24. I understand that the prosecution file history of the patent provides additional evidence of how both the Patent Office and the inventors understood the terms of the patent, particularly in light of what was known in the prior art. I understand that arguments and amendments made during prosecution may further require a narrow interpretation of a claim term, even if that term is used more broadly in the specification.

25. I understand that differences among claims can also be a useful guide in understanding the meaning of particular claim terms. For example, I am familiar with the doctrine of "claim differentiation" where the presence of dependent claims that add a particular limitation to an independent claim gives rise to a presumption that the limitation in question is not present in the independent claim.

B. Indefiniteness

26. I understand that the standard for indefiniteness is whether a person having ordinary skill in the art would understand what is claimed when the claim is read in light of the

specification and prosecution history. A claim is indefinite if, viewed in light of the specification and prosecution history, it fails to inform one skilled in the art about the scope of the invention with "reasonable certainty." The definiteness requirement must take into account the inherent limitations of language; reasonable certainty in light of the subject matter, and not absolute precision, is required.

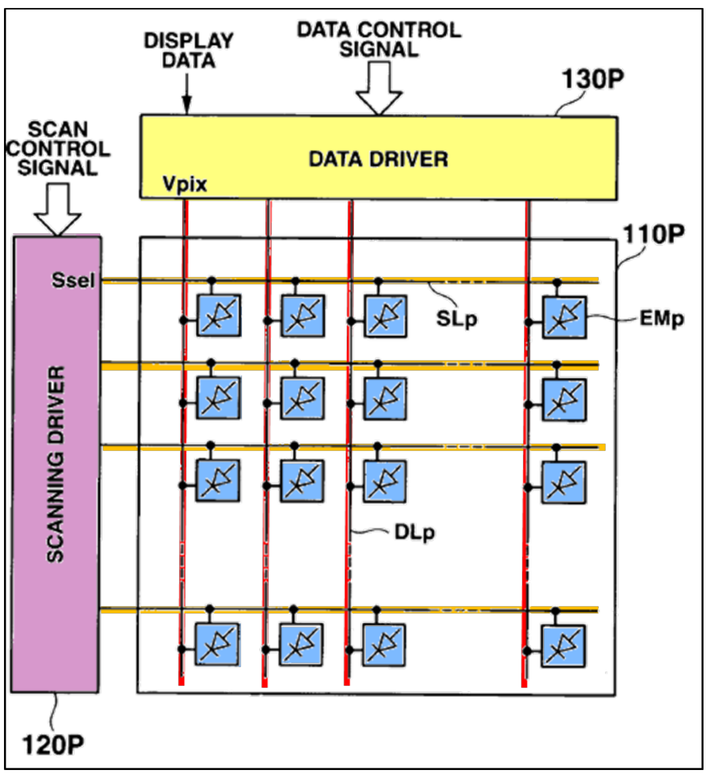
27. I understand that a patent must be precise enough to afford clear notice of what is claimed and apprise the public of what subject matter is still open to them in a manner that avoids a zone of uncertainty. I am informed that a claim does not provide clear notice of its scope if a claim term may be reasonably interpreted to refer to multiple different methods, which provide different results, and the intrinsic evidence offers no guidance regarding which method should be used.

28. I understand that indefiniteness is an invalidity defense, and that the defendant or accused infringer bears the burden to demonstrate a term is indefinite by clear and convincing evidence.

IV. TECHNOLOGY BACKGROUND

29. The Asserted Patents relate to flat panel organic light-emitting diode ("OLED") displays. *See* '615 Patent at 1:17-26; '042 Patent at 1:15-19; '068 Patent at 1:16-20. OLED displays are display panels made up of OLED pixels, arranged in a grid of rows and columns, which emit light to display an image. *See* '615 Patent at 1:40-59. OLED pixels contain organic electroluminescent (OEL) elements, which are made of organic materials that emit light when a current passes through them. The brightness of the OEL in an OLED pixel corresponds to the amount of current that is passed through it, becoming brighter as the current increases. *Id*. at 1:17-26.

30. The Asserted Patents specifically relate to one type of driving control circuit used to control OLED panels—Active Matrix ("AM") drive systems. *See* '042 Patent at 1:26-30, 1:44-58; '615 Patent at 2:4-10, Figs. 22-23; '068 Patent at 1:22-26. AM-OLED displays are devices that are able to control individual pixels through a pixel circuit associated with each individual pixel. *Id.*; *See also*, Ex. BB03 at 50-52. As can be seen in Figure 22 of the '615 Patent (annotated below), these pixel circuits (blue squares) are controlled by a data driver (yellow) and a scanning driver (purple), which jointly work together to select and control the pixel circuits. '615 Patent at 2:13-24; *see also* '042 Patent at 1:30-34, 1:44-58. The pixel circuits are connected to these drivers by scan lines (orange) and data lines (red), which respectively connect to the various rows and columns of pixels. *Id.*



'615 Patent at Fig. 22.

31. While all AM-OLED displays generally share the same panel structure, with the active-matrix circuits arranged in a rows and columns as depicted in Figure 22 above, the

internal structure of each of the individual pixel circuits contained therein often varies between different AM-OLED display panels. See, e.g., Ex. BB03 at 50-52. The pixel circuit of a traditional AM OLED panel, shown in Figure 23 of the '615 Patent (annotated below), contain two transistors and a capacitor.

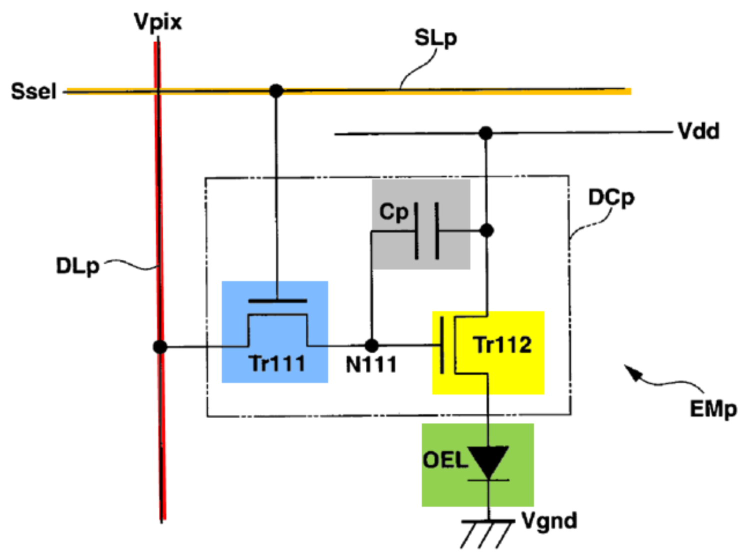


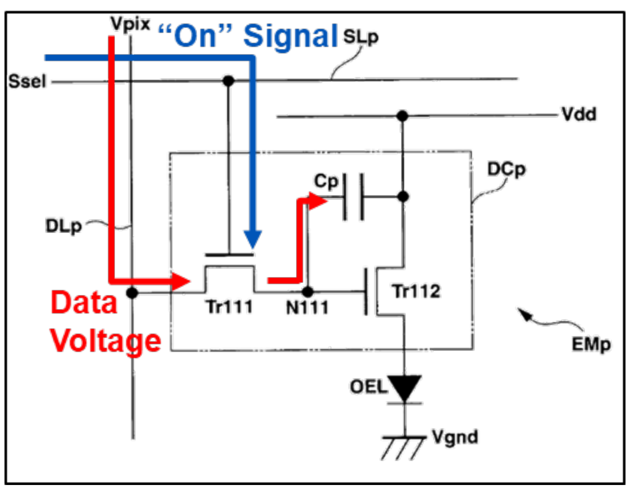
FIG.23
RELATED ART

'615 Patent at Fig. 23.

32. This pixel circuit contains a first transistor, known as a selection or switching transistor Tr111 (blue), which is controlled by a scan line SLp (orange). *See* '615 Patent at 2:25-41; *see also*, '068 Patent at 1:26-46; Ex. BB03 at 50-52; Ex. BB04. When the scan line SLp is selected and active (i.e., when voltage is high to turn the transistor on) it switches on the selection transistor Tr111; conversely, when the scan line SLp is not selected and inactive (i.e., when voltage is low to turn the transistor off), it switches off the selection transistor Tr111. *Id.*

33. In the figure above, the selection transistor Tr111 is connected to the data line DLp (red), which carries the image data voltage. *Id*. When the selection transistor Tr111 is switched on, image voltage data from data line DLp passes through Tr111; when the selection transistor Tr111 is switched off, image voltage data from data line DLp cannot pass through Tr 111. Within the pixel circuit, the selection transistor Tr111 is connected to the capacitor Cp (gray), which stores the image data voltage received from the data line DLp. *Id*. Both the selection transistor Tr111 and the capacitor Cp connect to and control a second transistor, known as the driving transistor Tr112 (yellow). *Id*. The capacitor Cp controls how much current flows through driving transistor Tr112 to the organic electro-luminescent (OEL) element (green). *Id*.

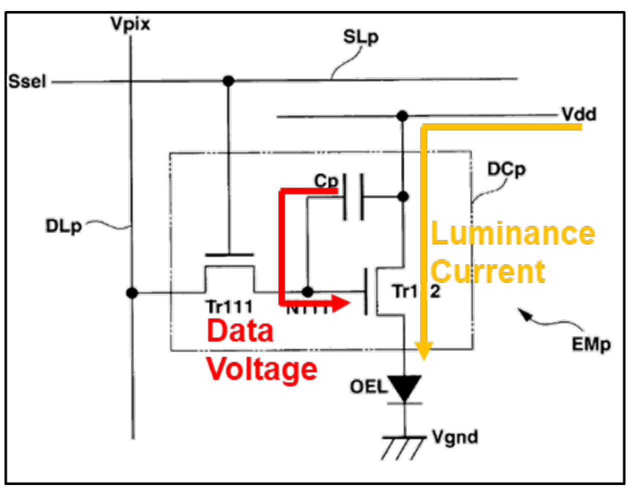
34. The traditional AM-OLED pixel circuit operates in a two phases or time periods. *See*, '615 Patent at 2:42-3:11; Ex. BB03 at 50-52; Ex. BB04. The first phase is sometimes called a write or programming period. During the first phase, as shown in Figure 23 of the '615 Patent (annotated below), a data voltage corresponding to a particular pixel luminance (i.e., brightness or intensity) is stored on the capacitor Cp in the pixel circuit. '615 Patent at 2:42-67.



35. For this to occur, an "On" signal is sent on the scan line SLp in order to turn on the switching transistor Tr111 (blue). *Id*. A data voltage (red) corresponding to the desired

OLED image luminance level is then applied on the data line DLp through the switching transistor Tr111, which in turn is written onto the storage capacitor Cp through Tr111 until the Tr112 gate voltage equals the data line voltage. *Id.* This process causes the capacitor to charge to the data voltage level, thereby storing this voltage at node N111. *Id.* This process is known as voltage programming, because the "voltage of the capacitor of each pixel circuit is set by a voltage signal." *See* Ex. JK01 at 1:49-2:2; *see also*, '068 Patent at 3:21-31; Ex. JK02 at [0005].

36. During the second phase, known as the driving or emission period (annotated below), the scan line SLp voltage is low and switching transistor Tr111 is off. '615 Patent at 2:57-3:20. As a result, the capacitor Cp discharges so that the voltage stored on capacitor Cp from the prior phase is applied to the gate of the driving transistor Tr112, turning it on. When the driving transistor Tr112 is turned on, it allows a luminance or driving current to flow from the source line (Vdd) through Tr112 to the common cathode (ground, Vgnd) of the OEL element. The OEL element will then emit light.

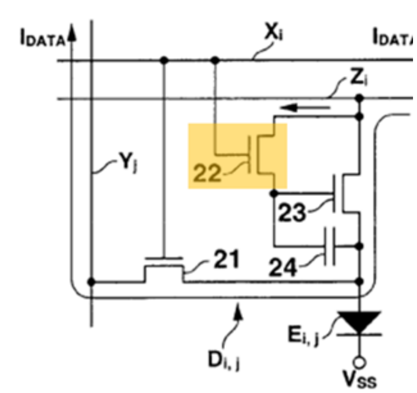
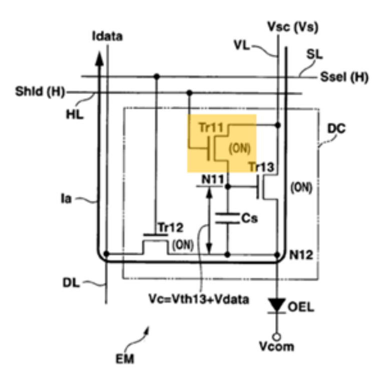
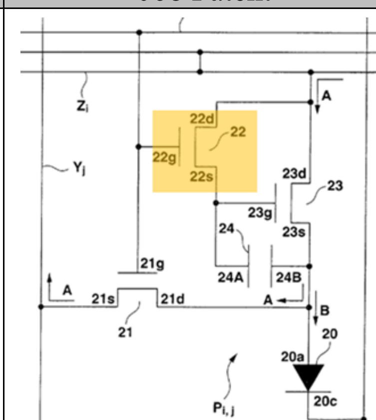


37. The magnitude of the driving current that flows through Tr112 determines the brightness or luminance of the OEL element. The magnitude of the luminance current, in turn, is controlled by the magnitude of the voltage that is applied to the gate of Tr112—the higher the applied voltage at the gate of Tr112, the higher the luminance current.

V. SUMMARY OF THE ASSERTED PATENTS

A. General Overview

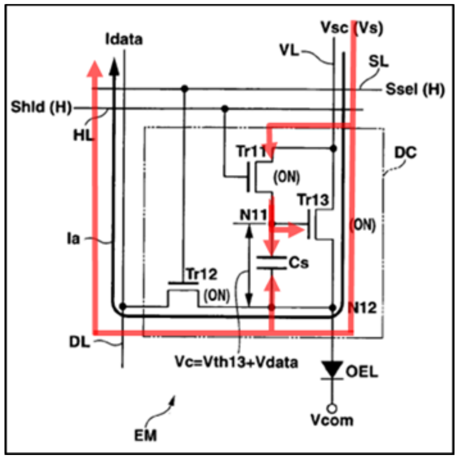
38. The three Asserted Patents share overlapping inventors, were originally assigned to Casio, and disclose many common features discussed in this section. All three patents describe purported problems that exist in the traditional two-transistor OLED pixel circuit that was described in the previous section. These problems arise because it can be difficult to accurately and reliably control the amount of current flowing through the OEL element—and therefore the brightness or luminance of the OLED pixels— based on a data voltage applied to the pixel circuit. For example, the ’042 Patent notes that “the channel resistance of a transistor changes in accordance with a change in ambient temperature, or changes when the transistor is used for a long time. . . . This produces variations in luminance on the display screen.” ’042 Patent at 2:7-28. The ’615 Patent also notes that issues with the traditional pixel circuit make it “difficult to stably realize the light emission operation at the appropriate luminance gradation sequence in accordance with the display data for a long time.” ’615 Patent at 3:35-63. To resolve these alleged problems, the asserted patents propose the use of a modified pixel circuit (annotated below) that includes an additional, third, transistor (orange).

’042 Patent	’615 Patent	’068 Patent
 Figure 7.	 Figure 4A.	 Figure 2.

39. Some of the Asserted Patents call this additional transistor the "hold transistor." *See, e.g.*, '615 Patent at 4:31-32; *see also*, '068 Patent at 7:10-11. The hold transistor allows for a reset or precharge operation to be performed after the switching transistor is turned on but before current programming is performed. See, e.g., '615 Patent at 19:34-47, 23:59-63; '042 Patent at 13:31-45. During this process, a reset or precharge voltage is applied on the data line and is stored in the capacitor, which the patents claim makes the subsequent current programming operation quicker and more accurate. *Id.*

40. The hold transistor is also involved in the threshold correction operation performed after the precharge operation is completed. According to the patent, this allows for correction of the drive transistor Tr13 allowing AM-OLED uniform light emission. '615 Patent 21:25-45.

41. Finally, the hold transistor is part of the writing operation after the threshold correction operation is completed. During this time period, as shown in the annotated figure below, the data current (red) is pulled through both the driving transistor Tr13 and the capacitor Cs. *Id.* at 23:2-19, 23:27-36. During this process, a voltage related to the data current is stored in the capacitor Cs, and is then applied to the gate of the driving transistor Tr13. *Id.* at 24:12-27. The ***current value*** of the data current, however, is held constant so that it remains proportional to the desired brightness level of the pixel. *Id.* This process results in a voltage level being stored on the capacitor Cs that matches the desired pixel brightness level, but that is calibrated to the individual properties of the driving transistor Tr13. *Id.*



’615 Patent Fig. 4A.

B. The ’615 Patent

42. The ’615 Patent is titled “Light emission drive circuit and its drive control method and display unit and its display drive method” and was filed on December 12, 2005. ’615 Patent at Cover.

43. The ’615 Patent is generally directed to an OLED “emission drive circuit and its drive control method.” ’615 Patent at 1:17-19.

44. Figure 1 (annotated below) shows the OLED pixel circuit of the ’615 Patent. As described above, this pixel circuit has a capacitor (orange) and three thin film transistors: the holding transistor Tr11 (green), the selection transistor Tr12 (purple), and the driving transistor Tr13 (blue). *See* ’615 Patent at 17:7-43. The switching transistor is turned on and off based on signals sent on the selection line SL (purple). *Id*. The holding transistor is turned on and off based on signals sent on the hold line HL (blue). *Id*.

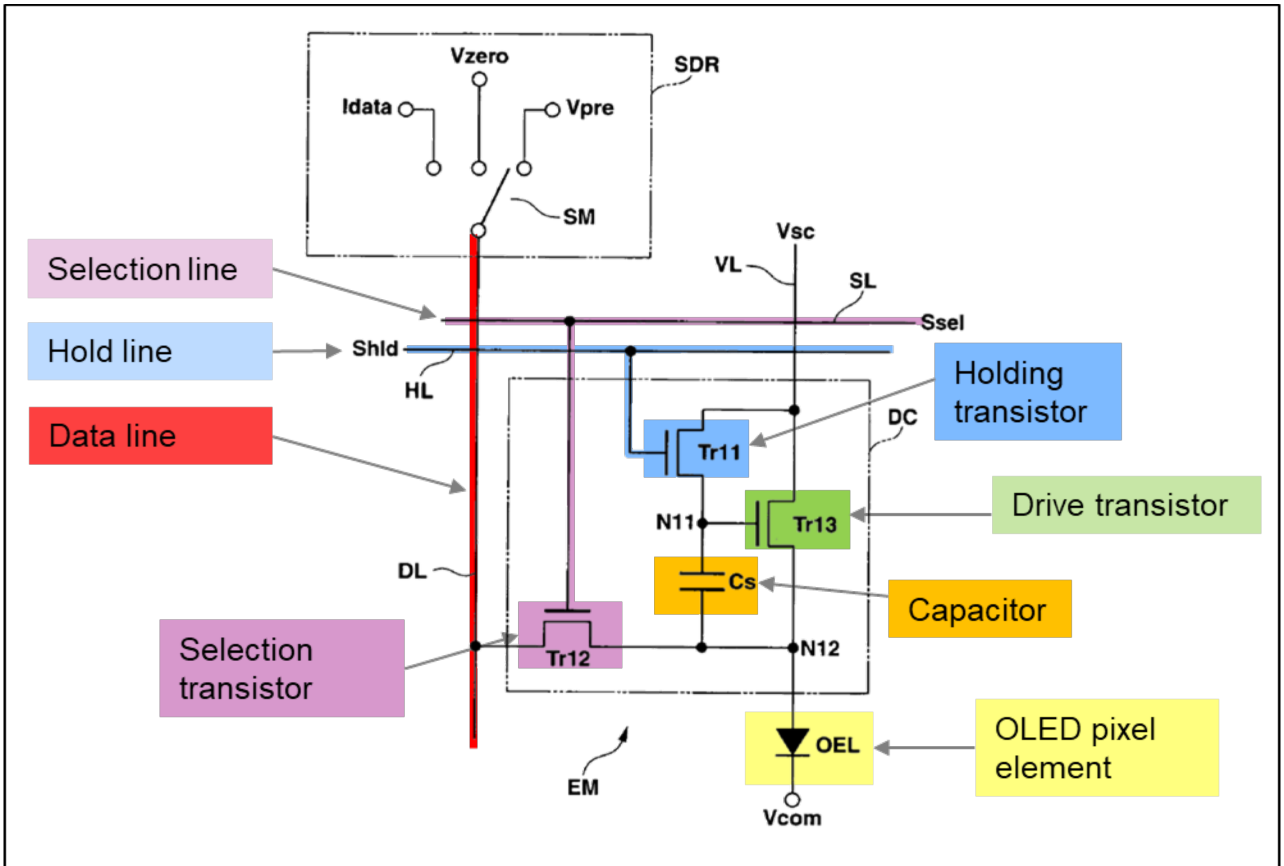


FIG.1

Id. at Fig. 1.

45. Figure 2 (annotated below), shows that the method for operating the '615 circuit occurs in four distinct "operation time periods": 1. the precharge operation period Tpre (red); 2. the threshold correction operation period Tth (blue); 3. the writing operation period Twr (green); and 4. the light emission operation period Tem (yellow). *See* '615 Patent at 18:37-3:9.

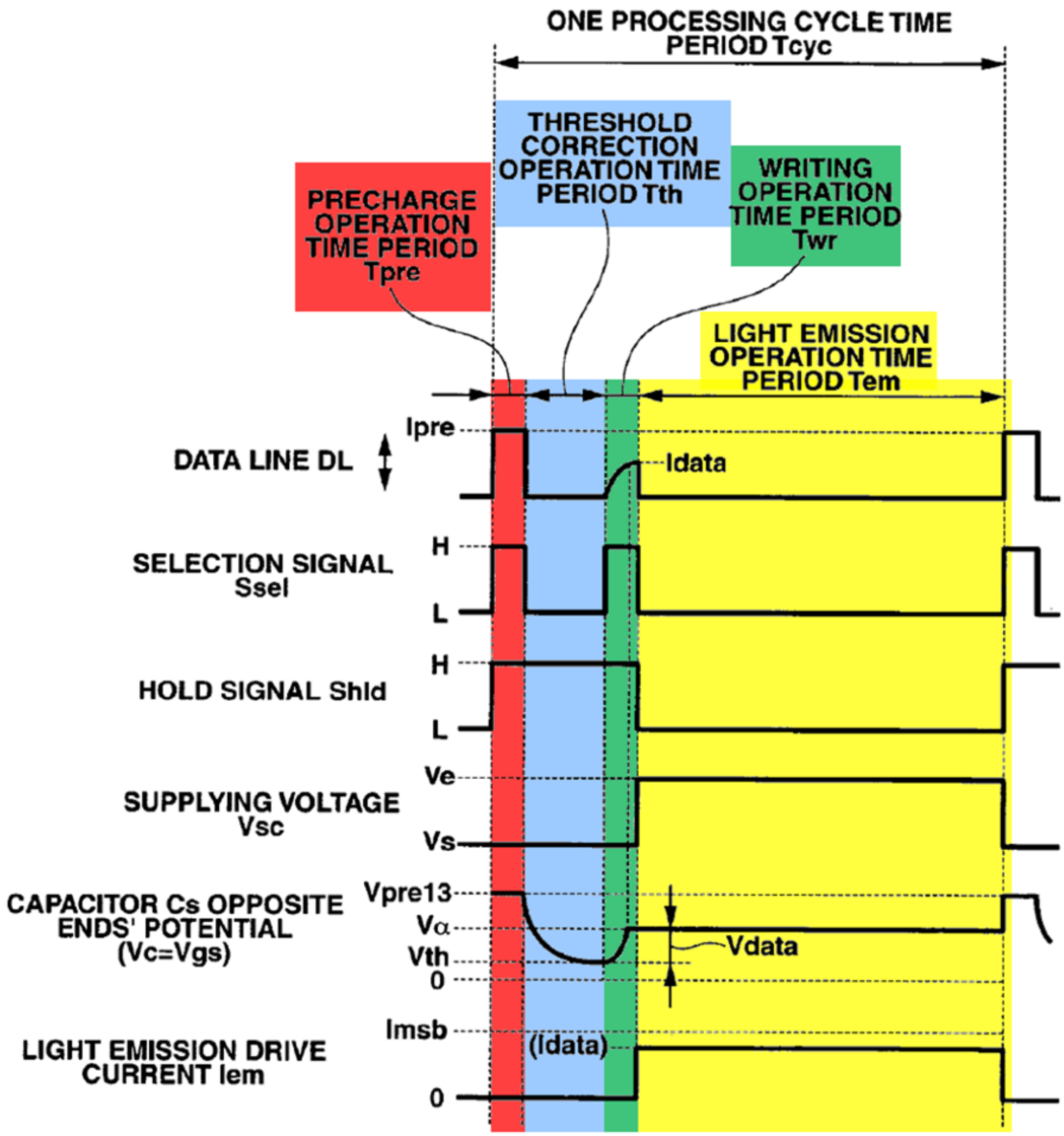


FIG.2

Id. at Fig. 2.

46. First, in the precharge operation period Tpre shown in Fig. 3A (annotated below), the selection transistor Tr12 and the hold transistor Tr11 are turned on. '615 Patent at 19:34-47. A "precharge voltage Vpre" (yellow) is then applied to the data line DL (red) by signal drive

circuit and a supply voltage Vsc (Vs) (gray) is applied on the voltage line VL (purple), causing a precharge current Ipre (green) to flow through the circuit from the supplying voltage line VL towards the signal drive circuit SDR between the drain and source of the drive transistor Tr13. *Id*. This results in "the electric charges corresponding to the potential difference Vc in accordance with the precharge current Ipre [to be] accumulated without delay [in] the capacitor Cs resulting in the drive transistor precharge voltage Vpre13," as shown in orange in Figure 3A below. *Id*. at 20:63-21:9.

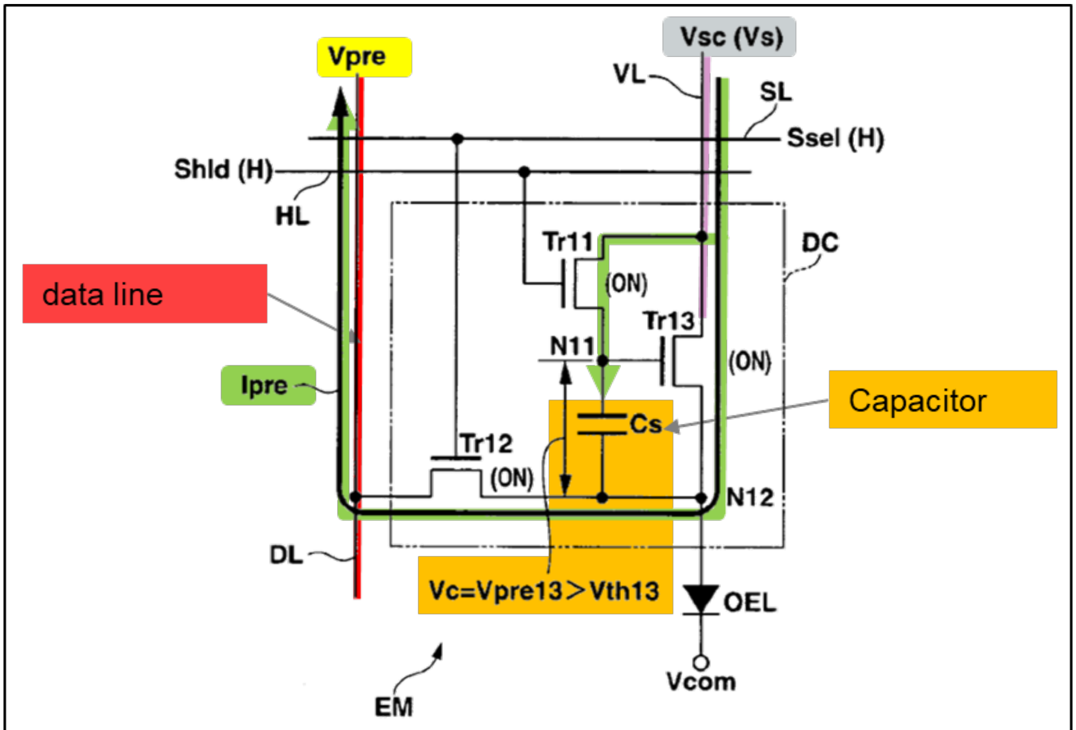


FIG.3A

47. As shown in annotated Figure 3A above, by the end of the precharge operation period, the voltage "Vc" across the capacitor Cs is equal to another "precharge voltage" called Vpre13, and both Vc and Vpre13 have voltage values greater than "Vth13." *Id*. at 20:63-66, 21:4-14. Vth13 is the threshold voltage of the drive transistor Tr13, meaning that to switch on

Tr13, a gate-to-source voltage greater than its threshold voltage Vth13 must be applied to Tr13. *Id.*

48. Second, in the threshold correction operation period Tth shown in Figs. 2 and 3B (annotated below), the selection transistor Tr12 is turned off, while the hold transistor Tr11 remains on. This disconnects the capacitor Cs and the contact point N12 from the data line DL. '615 Patent at 21:25-34. The drive transistor Tr13, meanwhile, is kept on (e.g. Vc>Vth13) by electrical charges accumulated in capacitor Cs during the precharge operation period. During this period, the source electrode voltage of Tr13 (the contact point N12) gradually increases until it approaches the voltage of the drain electrode of Tr13. This, in turn, decreases the gate-to-source voltage of Tr13 (called "Vgs") until it reaches the threshold voltage value, Vth13. During this time period, the electrical charges accumulated on capacitor Cs decrease, so that by the end of the threshold correction operation period, the voltage across the capacitor Cs (Vc) is equal to the threshold voltage Vth13 of the driving transistor Tr13. This is shown in Figure 3B below, which states that "Vc = Vth13."

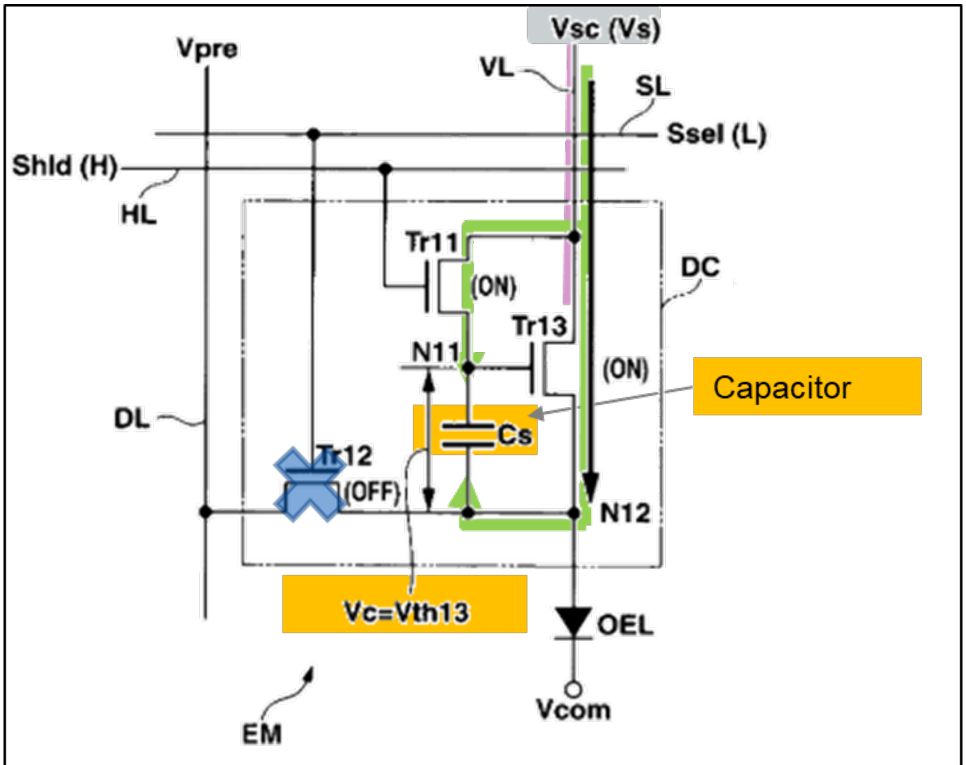


FIG.3B

49. Third, in the writing operation period Twr shown in Fig. 4A (annotated below), the selection transistor Tr12 is once again turned on while the hold transistor Tr11 continues to remain on. *See* '615 Patent at 23:27-36. A low voltage Vsc (Vs) (grey) continues to be applied on the voltage line VL (purple), and a constant "gradation sequence current" Idata (green) is generated by the signal drive circuit, SDR, resulting in Idata flowing through data line DL (red) from the supplying voltage line, VL, into SDR. *Id*. The current Idata is pulled through both the driving transistor Tr13 (blue) and the capacitor Cs (orange), causing a feedback loop to occur within the circuit. *Id*. This causes a voltage Vdata, which corresponds to the current Idata, to be added to the voltage Vth13 that was already stored in the capacitor Cs at the end of the prior threshold correction operation shown in Figure 3B above. *Id*. This new voltage stored on the capacitor (i.e., Vc=Vth13 + Vdata) corresponds to the luminance value desired to be produced by the OLED pixel OEL. *Id*. at 24:12-28.

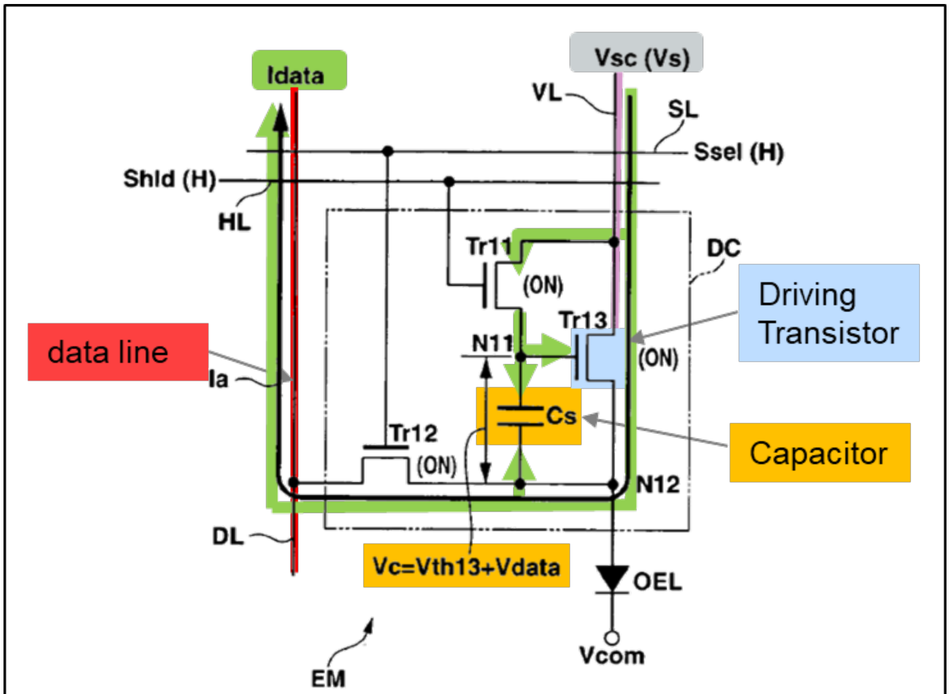


FIG.4A

50. Finally, in the light emission operation period Tem shown in Fig. 4B (annotated below), both selection transistor Tr12 and the hold transistor Tr11 are turned off. ’615 Patent at 24:43-58. A high driving voltage Vsc (Ve) (grey) is applied on the supply voltage line VL (purple) to the driving transistor Tr13 (blue). ’615 Patent at 25:46-26:2. This causes the light emission drive current Iem (green) to flow through the drive transistor to the OEL (yellow). *Id.* The value of this drive current Iem is proportional to the voltage Vc stored in the capacitor Cs (orange), which is applied to the gate of the driving transistor Tr13. *Id.* The flow of the light emission drive current Iem through OLED causes the OEL to light up with a luminance corresponding to its current value. *Id.*

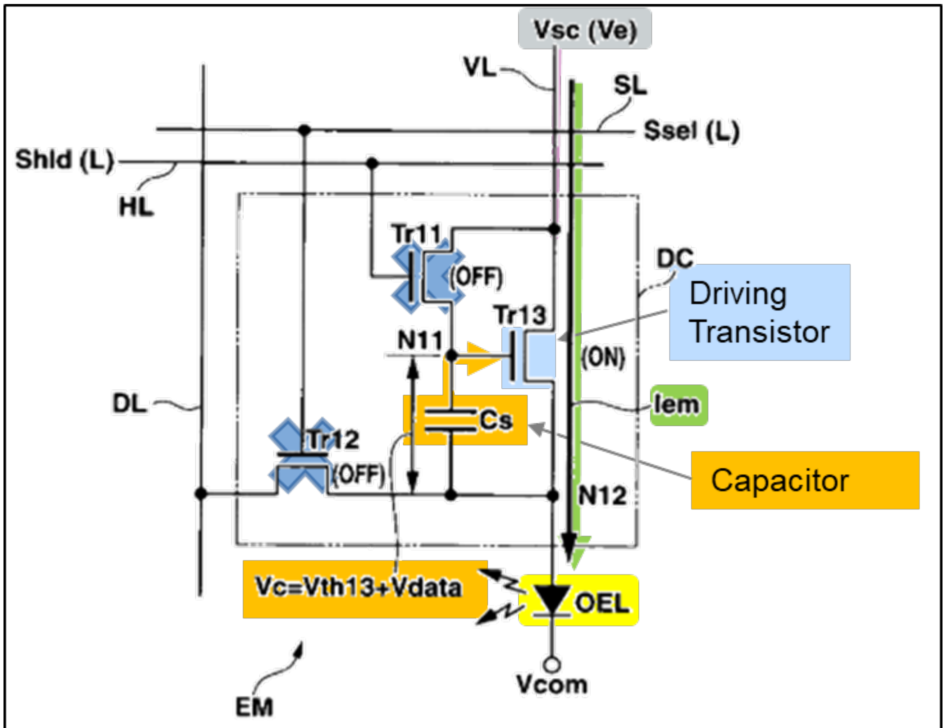


FIG.4B

VI. LEVEL OF ORDINARY SKILL IN THE ART

51. Based on my review of the asserted patents and claims, I believe a person of ordinary skill in the art around the time of the purported invention of the asserted patents have had a relevant technical degree in electrical engineering, computer engineering, physics, or the like, and 2–3 years of experience in active-matrix displays, such as AM-OLEDs, design and/or manufacturing.

52. In determining the level of ordinary skill in the art, I was asked to consider, for example, the type of problems encountered in the art, prior art solutions to those problems, the rapidity with which innovations are made, the sophistication of the technology, the educational level of active workers in the field, and the education and qualification of the inventors.

53. In light of the foregoing, I consider myself to be an expert in the field of flat panel displays and integrated circuits manufacturing, including thin film deposition techniques, etching

chemistry, chemical-mechanical polishing, devices and active-matrix circuits processing and photolithographic steps, and the designs used in the fabrication of devices and circuits, with the feature sizes ranging from micron to submicron for various industrial applications including FPDs, both now and by the time the patents were developed in 2004-2005. Therefore, I believe that I am qualified to provide an opinion as to what a person of ordinary skill in the art at the time of the invention ("POSITA") would have understood, known, or concluded regarding the subject matter of the '042, '068, and '615 Patents. My opinions concerning the Asserted Patents are thus from the perspective of a POSITA, as set forth herein.

VII. OPINIONS ON UNDERSTANDINGS OF ONE OF ORDINARY SKILL

A. "the operation"

54. In my opinion, the term "the operation" renders Claim 11 of the '615 Patent indefinite because it lacks antecedent basis and it is unclear from the rest of the claim or patent what "the operation" references or means.

55. The term "the operation" appears in the following limitation of Claim 11: "a voltage control section for controlling a drive voltage for making the light emission control section perform **the operation**, respectively."

56. There is no other reference in Claim 11 or any of its dependent claims (Claims 12 and 13) to any "operation" or similar phrase.

57. Although other limitations of Claim 11 refer to an "operation state" of a "writing control section" and a "voltage control section," the "operation state" is a different noun that, in the context of the claims, refers to a separate concept of the on/off state of the "writing control section" (which is a selection transistor Tr12 in the specification) and "voltage control section" (which is a holding transistor Tr13 in the specification). The "operation state" is thus completely unrelated to "the operation."

58. The ’615 Patent specification does not resolve the ambiguity of what is “the operation,” but only adds to the confusion. In fact, the specification refers to several distinct types of “operations”: (1) “precharge operation”; (2) “threshold correction operation”; (3) “writing operation”; (4) “light emission operation”; (5) “display operation”; (6) “gradation sequence display operation”; (7) “drive control operation”; and also just “operation” generically. ’615 Patent at 18:37-19:9, 23:20-33, 27:9-15; *see also id*. at 1:60-63.

59. For example, a passage at 18:37-19:9, excerpted below, summarizes the first four operations, which it refers to as “operation examples,” and also refers to another “operation” term, “drive control operation”:

> FIG. 2 is a timing chart showing a current value of the data line DL, a potential of a selection signal Ssel, a potential of a hold signal Shld, a potential of a supplying voltage Vsc, a potential difference between the opposite ends of a capacitor Cs, and a current value of a light emission drive current Iem flowing through the organic EL element OEL. FIGS. 3A and 3B are conceptual drawings showing the operation examples (***precharge operation/threshold correction operation***) of the light emission drive circuit according to the embodiment. FIGS. 4A and 4B are conceptual drawings showing the operation examples (***writing operation/light emission operation***) of the light emission drive circuit according to the embodiment.
>
> As shown in FIG. 2, the ***drive control operation*** of the light emission drive circuit according to the embodiment is carried out by setting the light emission drive circuit so as to include a ***precharge operation*** time period Tpre of accumulating a predetermined electric charge in the capacitor Cs of the light emission drive circuit DC, a ***threshold correction operation*** time period Tth of partially discharging the electric charges accumulated in the capacitor Cs of the light emission drive circuit DC in the ***precharge operation*** time period Tpre and remaining the electric charges equivalent to the threshold of the drain-to-source current Ids of the drive transistor Tr 13 in the capacitor Cs and holding the electric charges, a ***writing operation*** time period Twr of applying the gradation sequence signal in accordance with the display data via the data line DL and writing the electric charges in accordance with the display data in the capacitor Cs, and a ***light emission operation*** time period Tem of making the organic EL

> element to perform the ***light emission operation*** at the luminance gradation sequence in accordance with the display data on the basis of the electric charges accumulated in the capacitor Cs so that a predetermined precharge voltage Vpre is applied from the signal drive circuit SDR via the data line DL within one processing cycle Tcyc to acquire a gate-to-source voltage Vpre13 of the drive transistor Tr 13 (the absolute value of the voltage Vpre13 is larger than the absolute value of a gate-to-source voltage Vth13 of the drive transistor Tr 13. In an n channel transistor, the voltage Vpre13 is higher than the threshold voltage Vth13) (Tcyc≧Tpre+Tth+Twr+Tem).

Id. at 18:37-19:9.

60. The four "operation examples" are depicted in Figure 2, annotated as successive operations within the "one processing cycle time" in which a pixel is written and displayed.

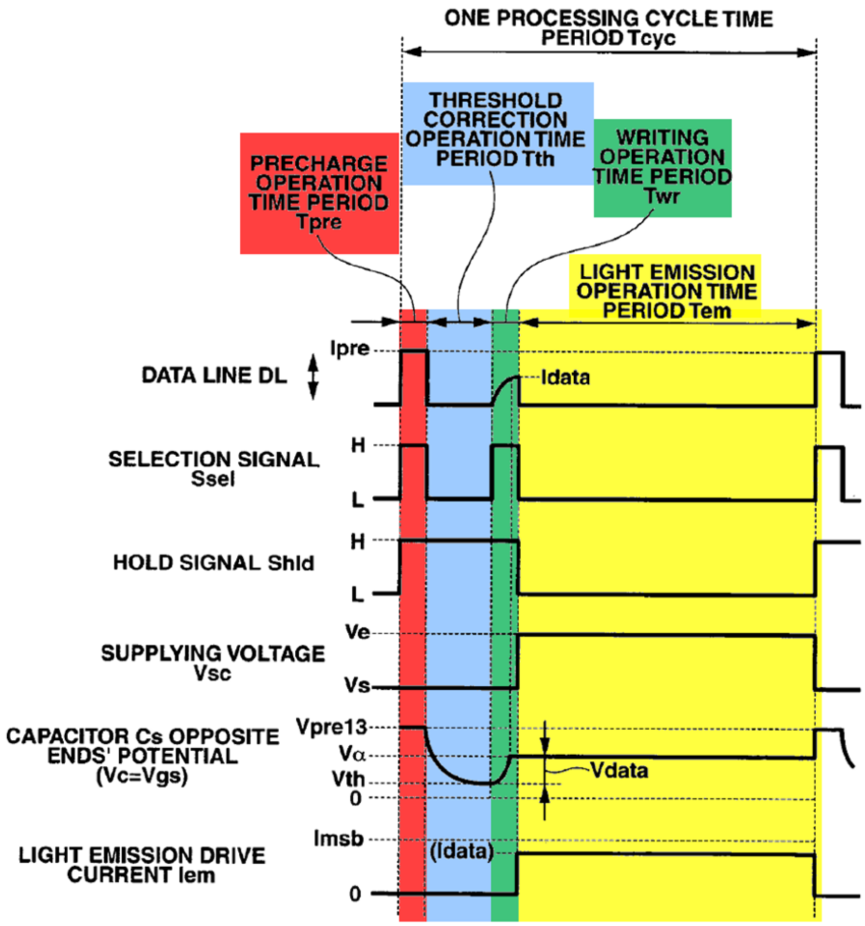


FIG.2

Id. at Fig. 2.

61. The other types of "operations" are referenced in the exemplary passages below:

- "display operation": "Therefore, when performing the ***display operation*** at the low luminance gradation sequence (when making the organic EL element OEL to perform the light emission operation at the low luminance gradation sequence), the current value of the gradation sequence current Idata to be supplied to the signal drive circuit SDR is made very small." *Id*. at 27:9-15.

- "gradation sequence display operation": "In this case, the normal gradation sequence display operation (the gradation sequence display for making the organic EL element OEL to perform the light emission operation) will be described and the no-light emission operation (the gradation sequence display operation so as not to make the organic EL element OEL to perform the light emission operation) will be described later." *Id*. at 23:20-26.

- "operation" (used alone):
  - "In such a light emission element type of display, various drive control mechanisms and control methods for controlling the operation of the light emission element (the light emission state) are suggested." *Id*. at 1:60-63.
  - "Thereby, when the selection transistor Tr 12 is turned on and ***the operation*** to drain the gradation sequence current Idata via the data line DL is carried out, the voltage of the potential further lower than the low voltage of the supplying voltage Vsc (=Vs) is applied to the contact point N12 (the source terminal of the drive transistor Tr 13 and the other end side of the capacitor Cs)." *Id*. at 23:27-33.

62. In view of the many types of distinct and very different "operations" described in the specification, a POSITA looking at Claim 11 could not discern with any reasonable certainty the meaning or scope of "the operation." For example, a POSITA looking at Claim 11 could not know which one, more than one, or none, of the several "operations" in the specification is being referenced by "the operation" in the claim. Similarly, a POSITA would not know which "operation" the "display unit" and its many sections and components are purportedly "perform[ing]" as required Claim 11. This lack of clarity is only compounded by the complete lack of antecedent basis for the term "the operation." Thus, "the operation" renders Claim 11 and its dependent claims indefinite.

63. I understand that Plaintiff Solas contends that "the operation" is not indefinite, but instead refers to steps recited earlier in Claim 11 of "generating a light emission drive current having a predetermined current value in accordance with the electric charges accumulated in the electric charge accumulating section and supplying the light emission drive current to the light emission element." But Solas's selection of this phrase as corresponding to "the operation" appears arbitrary and without basis. It is unclear why "the operation" should refer to the prior steps that Solas proposes, particularly when those prior steps include at least two separate "operations" of "generating a light emission drive current . . ." and "supplying the light emission

drive current." To the extent Solas later provides any bases for its proposal in its opening claim construction brief and supporting materials, I reserve the right to submit a supplemental declaration to address those bases.

B. "precharge voltage"

64. In my opinion, the term "precharge voltage" as used in Claim 11 of the '615 Patent, does not have a meaning or scope that a POSITA would understand with reasonable certainty in light of the intrinsic evidence. As detailed below, the '615 Patent specification discloses two different types of voltages that it calls a "precharge voltage," each with very characteristics, and Claim 11's use of the term make it unclear which (if any) "precharge voltage" in the patent is being referenced in the claim.

65. As context and discussed above, the '615 Patent describes four operation steps that are performed in writing and displaying a pixel value on a given pixel circuit. The first step is a "precharge operation" where a precharge voltage is applied on the data line "DL" to the pixel circuit. The precharge voltage applied to the data line is called "***Vpre***." As the specification explains: "the selection transistor Tr 12 is turned on and ***the data line DL to which the precharge voltage <u>Vpre</u> is applied*** electrically communicates with the source of the drive transistor Tr 13 and the other end of the capacitor Cs (the contact point N12) via the selection transistor Tr 12."). '615 Patent at 20:38-44.

66. When the precharge voltage Vpre is applied, it causes a separate "precharge voltage," called "***Vpre13***," to apply across the capacitor Cs. As the specification explains:

> . . . the electric charges accumulated in the capacitor Cs so that a predetermined ***precharge voltage Vpre*** is applied from the signal drive circuit SDR via the data line DL within one processing cycle Tcyc to ***acquire a gate-to-source voltage Vpre13*** of the drive transistor Tr13 (the absolute value of the voltage Vpre13 is larger than the absolute value of a gate-to-source voltage Vth13 of the

> drive transistor Tr13. In an n channel transistor, the voltage Vpre13 is higher than the threshold voltage Vth13.

Id. at 19:1-9.

> [T]he potential difference ***<u>Vpre13</u>*** that is larger than the threshold Vth13 of the drive transistor Tr 13 ***is applied to the opposite ends of the capacitor Cs*** (namely, between the gate and the source of the drive transistor Tr 13). Thereby, the precharge current Ipre of the large current in accordance with this drive transistor ***precharge voltage Vpre13*** compulsorily flows from the supplying voltage line VL toward the signal drive circuit SDR between the drain and the source of the drive transistor Tr 13.

Id. at 20:63-21:4.

67. The specification depicts both types of precharge voltage Vpre (red) and Vpre13 (blue) in its Figure 3A, annotated below:

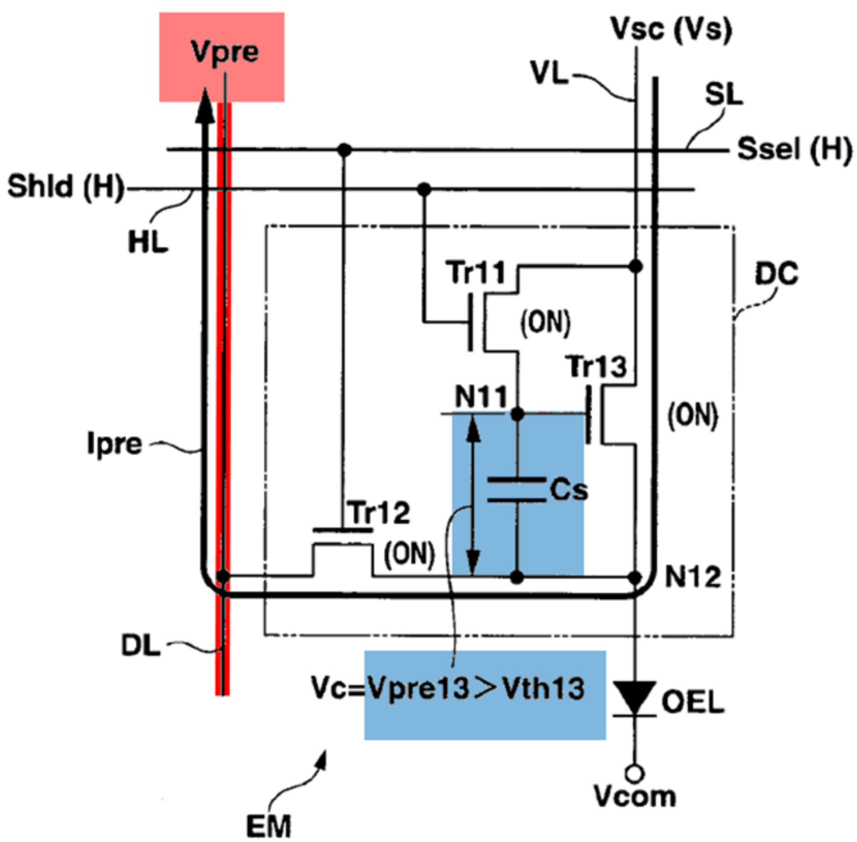


FIG.3A

68. As depicted in Figure 3A and described above, the two precharge voltages exist in different parts or locations of the pixel circuit. In particular, the precharge voltage Vpre is applied to the data line DL (red vertical line). *Id*. at 20:38-44. By contrast, the separate precharge voltage Vpre13 is formed across the capacitor Cs (blue region between point N11 and N12). *Id*. at 19:1-9, 20:63-21:4.

69. As also depicted in Figure 3A and described in the specification, the values of the two precharge voltages are very different. As Figure 3A shows, the precharge voltage Vpre13 across capacitor Cs must be greater than Vth13, which is the threshold voltage of the driving transistor Tr13. The specification confirms, stating: "the absolute value of the voltage Vpre13 is larger than the absolute value of a gate-to-source voltage Vth13 of the drive transistor Tr 13. In an n channel transistor, the voltage ***Vpre13 is higher than the threshold voltage Vth13***" and "the potential difference ***Vpre13 that is larger than the threshold Vth13*** of the drive transistor Tr 13 is applied to the opposite ends of the capacitor Cs." *Id*. at 19:5-9, 20:63-65, 23:64-66.

70. By contrast, the precharge voltage Vpre (applied to the data line) is not required to be greater than the threshold voltage of the transistor Tr13. The precharge voltage Vpre's value is specified by an equation in the specification, shown below:

> Here, the precharge voltage Vpre to be applied to the data line DL from the signal drive circuit SDR in the precharge operation time period Tpre is set so as to meet the following equation (1):
>
> $|Vs-Vpre|>Vth12+Vth13 \qquad (1)$

Id. at 20:44-49.

71. In this equation (1), there is no requirement that Vpre be greater than the driving transistor's threshold voltage, Vth13. In fact, the equation suggests nearly the opposite requirement. Rather than being greater than Vth13, the precharge voltage Vpre must have a value small enough that, even when subtracted from another voltage "Vs" ("selection voltage"),

the resulting difference is still greater than the threshold voltage Vth13, plus another threshold voltage Vth12 (which is the threshold voltage of the selection transistor Tr12).

72. The ’615 Patent’s asserted claims use the term “precharge voltage,” but in way that confuses the two distinct types of “precharge voltages” in the specification and improperly treats them as one and the same voltage. Specifically, asserted Claim 11 recites: “the data driver applies a precharge voltage exceeding a threshold value of the drive transistor to the data line.” This recitation requires that the recited “precharge voltage” have two characteristics. First, the “precharge voltage” must be applied by the “data driver” to the “data line.” Second, the “precharge voltage” must “exceed[] a threshold value of the drive transistor.”

73. There is no single “precharge voltage” in the ’615 Patent specification that has both of the two characteristics recited in Claim 11 — *i.e.*, (1) being applied to a “data line” and (2) exceeding a threshold value of the drive transistor. Instead, as discussed above, each of these two characteristics is attributable to only one of two separate and distinct “precharge voltages” Vpre and Vpre13 in the specification. Specifically, the first characteristic of being applied to a “data line” is ***only*** attributable to the precharge voltage “Vpre” in the ’615 Patent specification. As discussed, precharge voltage Vpre is applied to the data line DL; but the other precharge voltage Vpre13 is not applied to the data line DL as it instead applies across the capacitor Cs. And the second characteristic of exceeding a threshold value of the drive transistor is ***only*** attributable to the other precharge voltage Vpre13. As discussed, Vpre13 is greater than the threshold voltage of the drive transistor, Vth13; but the other precharge voltage Vpre is not necessarily greater and the specification suggests that it is instead a relatively small value.

74. Claim 11 thus conflates the two distinct “precharge voltages” and improperly treats them as a single “precharge voltage.” But because there is no such single “precharge

voltage" in the specification — that is both applied to the data line and greater than the threshold value of a drive transistor — a POSITA would not understand the meaning, scope, and bounds of the "precharge voltage" recited in Claim 11, thus rendering Claim 11 and its dependent claims indefinite.

VIII. OTHER COMMENTS

75. My opinions are subject to change based on any expert opinions that Solas may later present and information I may receive in the future or additional work I may perform. With this in mind, based on the analysis I have conducted and for the reasons set forth above, I have reached the conclusions and opinions in this Declaration.

76. I understand that the Court does not generally hear expert testimony during the claim construction hearing. However, if I am called to testify, in connection with my anticipated testimony in this action, I may use as exhibits various documents produced in this case that refer or relate to the matters discussed in this Declaration. I have not yet selected the particular exhibits that might be used. In addition, I may create or assist in the creation of certain demonstrative evidence to assist me in testifying, and I reserve the right to do so, to further support the positions in this Declaration.

77. I declare under penalty of perjury, under the laws of the United States, that the foregoing is true and correct.

Dated: June 25, 2020

Dr. Jerzy Kanicki